

### **Amendments to the Specification:**

Please replace the paragraph beginning on page 2, line 10, with the following amended paragraph:

Fig. 1(c) shows the transmission characteristic for a high-frequency signal ~~from point 1~~ ~~point 2~~ for layer thicknesses varying by 10%. The transmission characteristic changes with thickness; in particular the resonant frequency is shifted.

Please replace the paragraph beginning on page 2, line 25, with the following amended paragraph:

According to a preferred refinement, a second ground electrode may be provided, the ~~plane comprising common plane with the~~ capacitor electrode and line being arranged parallel to said second ground electrode at a distance  $h_2$ . The ~~plane comprising common plane with the~~ capacitor electrode and line lies between the first and second ground electrodes.

Please replace the paragraph beginning on page 2, line 30, with the following amended paragraph:

According to the invention, in a multilayer stack having a metallization structure as defined ~~above~~ above, it is also provided that this metallization layer is arranged on a dielectric layer, the dielectric constant  $\epsilon_{\text{medium}}$  of which is greater than the dielectric constant  $\epsilon$  of the surrounding dielectric layers. “Surrounding layers” means the layers adjoining the layer having the dielectric constant  $\epsilon_{\text{medium}}$ . The dielectric constant of such surrounding layers is represented by  $\epsilon$ , and the thickness of such surrounding layers is represented by  $d_\epsilon$ . It has been found that, in such an arrangement, variations in the layer thickness of the dielectric layer having the dielectric constant  $\epsilon_{\text{medium}}$  only very slightly affect the transmission characteristic or the shift in resonant frequency. If, specifically within the dielectric layer, the layer thickness decreases, the capacitance of the capacitor

is increased. At the same time, the metal line is located closer to the ground electrode. This line acts as a coil. At the ground electrode, mirror currents are induced which lower the inductance of the line. The closer the line is to the ground electrode, the lower the inductance of the line. The product of capacitance and inductance thus remains approximately constant and hence so does the resonant frequency

$$f = \frac{1}{2\pi\sqrt{L \cdot C}}$$

of the circuit. Inversely, when the layer thickness increases the capacitance of the capacitor becomes smaller, while the inductance of the line becomes greater. As a ~~result~~ result, the product LC again remains approximately constant.

Please replace the paragraph beginning on page 4, line 3, with the following amended paragraph:

Fig. 1(a) shows a diagram of a conventional series resonant circuit.

Please replace the paragraph beginning on page 4, line 4, with the following amended paragraph:

Fig. 1(b) shows the three-dimensional design of the conventional series resonant circuit of Fig. 1(a).

Please replace the paragraph beginning on page 4, line 6, with the following amended paragraph:

Fig. 1(c) shows that transmission characteristic of the conventional series resonant circuit of Fig. 1(a) in the case of variation of the thickness of the dielectric layer by  $\pm 10\%$ .

Please replace the paragraph beginning on page 4, line 27, with the following amended paragraph:

FIG. 2 shows an example of embodiment of a multilayer stack according to the present invention, which is made up of a number of dielectric layers 10, 12, 14, 16, 18, where the dielectric layer 14 on a ground electrode 30 has a dielectric constant which is greater, for example by a factor of 2, than the dielectric constants of the surrounding layers 12, 16. The thickness  $d_{\text{medium}}$  of the dielectric layer 14 is smaller than that of the surrounding dielectric layers 12, 16 and, in order to keep the interaction with surrounding structures low, the layer thickness  $d_{\text{medium}}$  should advantageously be small compared to the distances to adjacent structures, while  $\epsilon_{\text{medium}}$  on the other hand should be as great as possible. It is thus possible for capacitors having sufficiently small dimensions to be integrated. A metallization structure 20 is arranged at the interface between the dielectric layer 14 and the dielectric layer 12, ~~said the~~ metallization structure being composed of a capacitor electrode 22 and a line 24 that partially surrounds the ~~latter~~ capacitor 22. In the illustrated embodiment, w designates the width of the line 24, and  $h_1$  designates a distance between the metallization structure 20 and the ground electrode 30. Also, in the illustrated embodiment, the ratio of the width w of the line 24 to the distance  $h_1$  is greater than 3. In the particular embodiment illustrated in FIG. 2, for the layer 14,  $d_{\text{medium}} = 25\mu\text{m}$ , and  $\epsilon_{\text{medium}} = 20$ . (Also in the particular embodiment illustrated in FIG. 5a, for the layer 14,  $d_{\text{medium}} = 25\mu\text{m}$ , and  $\epsilon_{\text{medium}} = 20$ .) For adjoining layers 10, 12, 16 and 18 above and below,  $d = 100\mu\text{m}$  and  $\epsilon = 10$ .

Please replace the paragraph beginning on page 5, line 4, with the following amended paragraph:

Fig. 3 shows the three-dimensional design of the series resonant circuit ~~structure~~ structure 20 with the capacitor electrode 22, the line 24, and supply lines 26 ~~supply lines~~. The supply lines 26 connect to the line 24.

Please replace the paragraph beginning on page 5, line 8, with the following amended paragraph:

The transmission of power in the circuit according to the invention is shown in Fig. 4. It can clearly be seen that variations of, for example, +10% and -10% in the layer thickness of the dielectric layer 14 lead only to a very slight change in the resonant frequency or in the overall filter curve.

Please replace the paragraph beginning on page 5, line 10, with the following amended paragraph:

The electrical response of the circuit according to the invention has great stability with respect to interaction with other metallizations which are located in the multilayer stack above and below the series resonant circuit. In the multilayer stack of FIG. 2, above the dielectric layer 12 there is no ground electrode above the metallization structure 20. FIG. 5(a) shows the design of this structure with an additional ground electrode 32 above the metallization structure ~~20~~; 20, in addition to the ground electrode 30 below the metallization structure 20. The illustrated metallization structure 20 includes the capacitor electrode 22 and the line 24, as described above. In the illustrated embodiment,  $w$  designates the width of the line 24,  $h_2$  designates a distance between the metallization structure 20 and the additional ground electrode 32, and the ratio of the width  $w$  of the line 24 to the distance  $h_2$  is greater than three. FIG. 5(b) shows the transmission characteristic, where without a ground electrode (curve I) and at different distances of the additional ground electrode of 100  $\mu\text{m}$  (curve II) and 200  $\mu\text{m}$  (curve III) practically no variations in the resonant frequency can be seen. This effect is based on the high degree of coupling of the ~~structure~~ metallization structure 20 according to the invention to the ground electrode 30 (see Fig. 5(a)) arranged at a small distance and the advantageously relatively high dielectric constant compared to that of the surrounding layers.

Please replace the paragraph beginning on page 5, line 26, with the following amended paragraph:

Fig. 7 shows a multilayer stack having two ground electrodes 30, 32, between which the metallization structure 20 is arranged, where between the metallization structure 20 and the ground electrodes 30 and 32 in each case dielectric layers 14 and 14', respectively, having increased dielectric constants compared to that of the surrounding layers 12, 16 are provided. Otherwise, the multilayer stack corresponds essentially to that of Fig. 2, having other similar dielectric layers 10 and 18, as described above. Additionally, the metallization structure 20 includes a capacitor electrode 22 and a line 24, as described above. In the illustrated embodiment, for the layers 14 and 14',  $d_{\text{medium}} = 25\mu\text{m}$ , and  $\epsilon_{\text{medium}} = 20$ .